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COMPUTERIZED TRAINING SYSTEM

GTE Sylvania, Incorporated
Needham Heights, Massachusetts

15 October 1976

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PROJECT ABACUS

Report CTD-TR-76-4

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COMPUTERIZED TRAINING SYSTEM
FINAL REPORT

Prepared by:

GTE-Sylvania Inc.

15 November 1976

Approved for public release:
Distribution unlimited.

Prepared for:
U.S. Army Computer System
Support and Evaluation Agency
Pentagon, Washington, DC 20310

SOLDIER COMMUNICATORS
FORT GORDON
HOME OF THE SIGNAL CORPS

NOTICES

This report has been reviewed and is approved.

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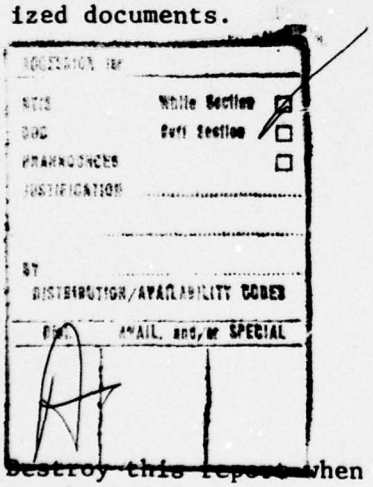

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The Project ABACUS computer system was tested for acceptance by the government on 23-27 February 1976, 22-23 March 1976 and 19-30 July 1976. This report describes the actions taken by the contractor, GTE-Sylvania, Inc. to correct the problems uncovered during the Phase III Acceptance Test conducted 19-30 July 1976.

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FINAL REPORT

Computerized Training System

Contract No. DAHC26-74-C-0006

26 December 1973 - 15 October 1976

Prepared for:

U.S. Army Computer System

Support and Evaluation Agency

Prepared by:

GTE - Sylvania

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FOREWORD

The Project ABACUS Computer System was tested for acceptance by the government on 23-27 February 1976, 22-23 March 1976, and 19-30 July 1976. This report desribes the actions taken by the contractor, GTE-Sylvania, Inc. to correct the problems uncovered during the Phase III Acceptance Test conducted 19-30 July 1976.

ROBERT S. FOSTER
LTC, SigC
Project Director,
Project ABACUS

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1.0 Introduction

This document, submitted in accordance with Item 5AH, Contract DAHC-26-74-C-006, Computerized Training System, reports the corrective actions taken by GTE Sylvania to correct problems uncovered during Phase III Testing of CTS at Ft. Gordon, Ga. The tests were conducted during the period 19 July through 30 July, 1976. The findings of these tests are reported in the Army Test and Evaluation Report dated 12 August 1976. Corrective actions taken by GTE Sylvania were performed over the period 2 August through 25 September 1976. Verification tests performed by Army CTS and GTE Sylvania personnel took place during the period 27 September through 8 October 1976. All corrections to problems cited in the Army Test and Evaluation Report were found by Army test personnel to be satisfactory. The effort of Lt. David Wickert, Army CTS Test Administrator, contributed greatly to the analysis of software test problems, and implementation and test of corrections made.

2.0 General Software Modifications

This section describes the CTS software activity from the end of the Phase III acceptance test, July 19-30, 1976, through October 8th. The principal results of the Phase III tests indicated a weakness in the DEC RSX-11D Version 4A operating system and occasional halts in the DC software. These conditions Occured while the system was under a user load of just over 100 students. The RSX-11D problem was caused by peak SC activity that would fill the RSX-11D node pool (dynamic memory scratch area) and subsequently cause the SC to crash. Attempts to generate a new RSX-11D system with a larger node pool failed due to errors in the DEC system generation procedure. DEC would not fix the problem because they no longer supported RSX-11D version 4A. As a result the SC operating system was upgraded to RSX-11D Version 6B. Some modifications were made to the SC routines and all programs were recompiled and retask built for operation under 6B. The new version was then tested successfully.

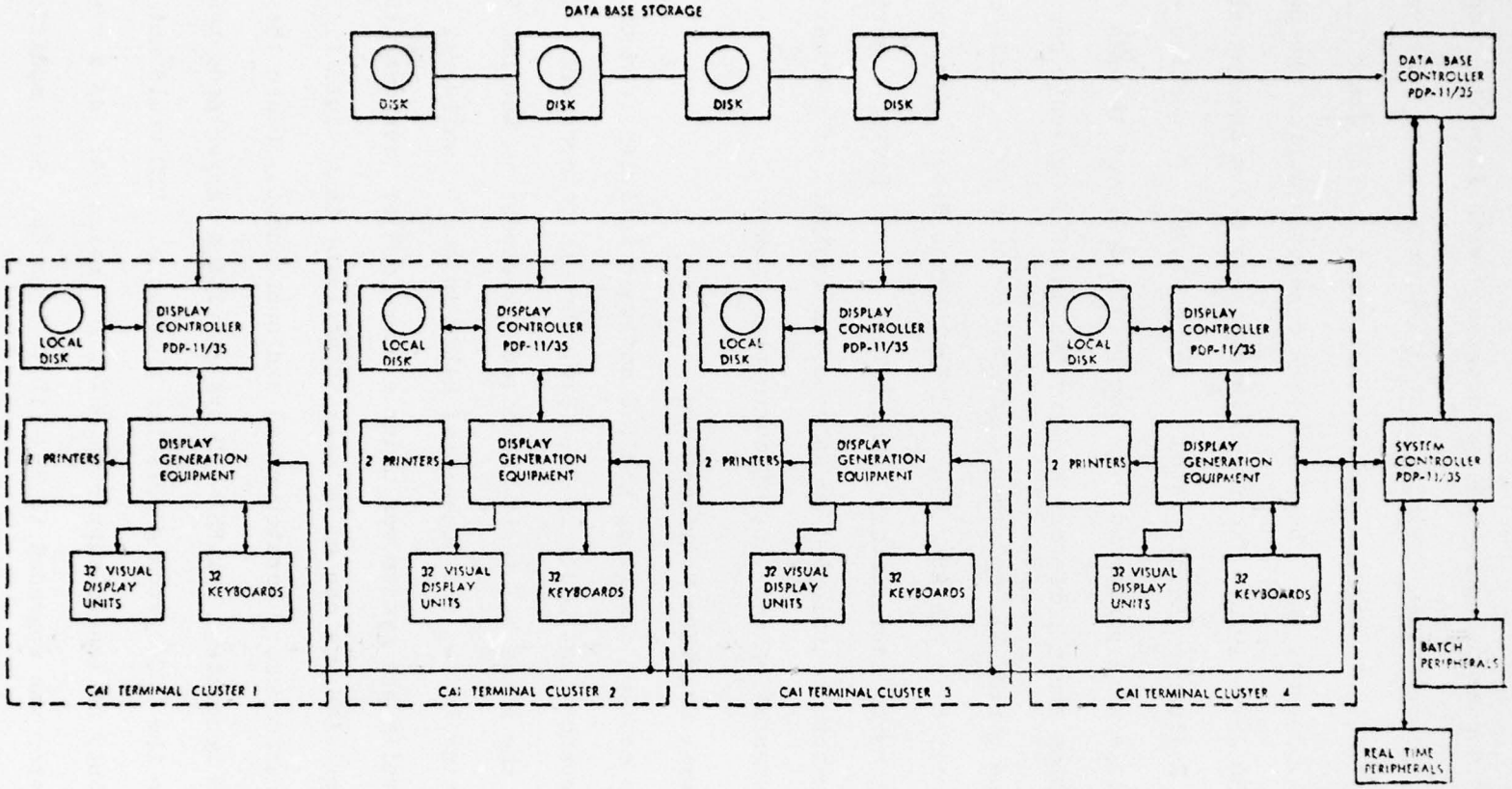

Figure 1-1. Block Diagram of Computerized Training System

The balance of the CTS was delivered to Fort Gordon in early May 1975. The delivery consisted of the System Controller and peripheral devices, the Data Base Controller, three Display Controllers and 96 terminals. All the equipment at Fort Gordon was integrated into one 128-terminal system. With the equipment was delivered all of the system software including DEC's RSX-11D real time operating system and GTE Sylvania's System Control, Display Control, Data Base Control, System Readiness Check, Initial to Final System File Conversion and CLASS I Language programs.

During the Spring of 1975, an installation study was performed to determine an effective and economical method of implementing the Army's installation plan. The Installation Study Technical Report was delivered in June 1975.

In July 1975 the contract was modified to add further installation tasks. This work was completed in February 1976 and the final Acceptance Test completed in October 1976.

3.0 CTS Hardware

3.1 Display Controller Subsystem

The Display Controller Subsystem consists of a PDP 11/35-FL computer, a peripheral disk, display generation equipment and 32 CTS terminals. The 128 terminal system installed at Fort Gordon has four display Controller subsystems, each with 30 student and two instructor terminals. A block diagram of a CTS Display Controller (DC) is shown in Figure 3-1. Two features unique to GTE Sylvania's system are the dual bus structure for the DC and the method used to generate random graphics.

3.1.1 DC Dual Bus Structure

Most display systems interface the terminals with the computer over a low speed communications link, i.e, baud rates between 110 and 2400. This interface is satisfactory for transmitting operator generated keyboard input since the rate at which that input is generated is limited by the operator's typing speed. However, such low speed links are not suitable for transmitting the large amount of data required for a display. In the CTS application up to 3804 words are needed, depending on the display complexity, to define the contents of the display screen. With 32 terminals in each display cluster competing for service and with

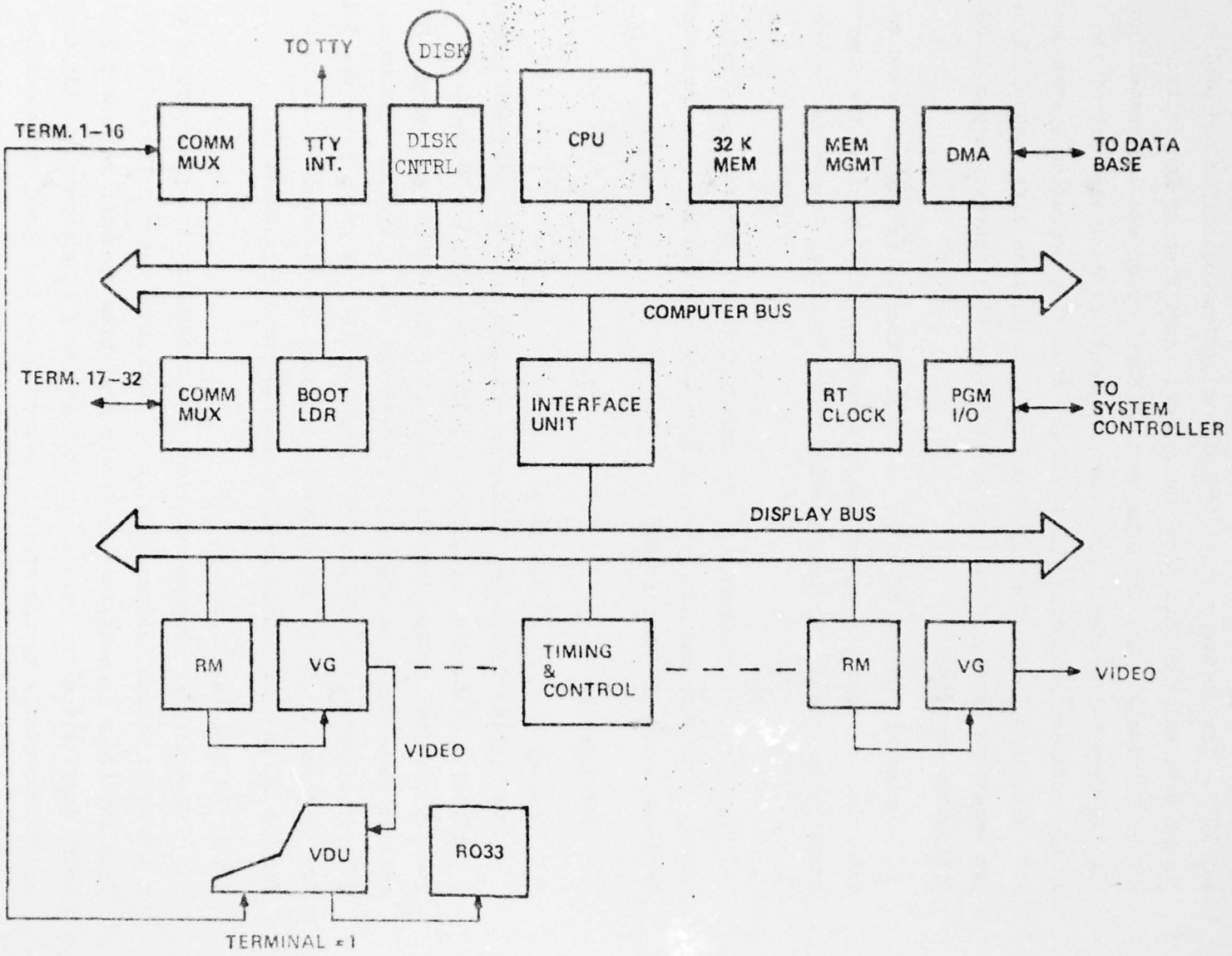

Figure 3-1 CTS Display Controller Subsystem

relatively low speed communications interfaces, the overhead time required to service all terminals would be considerable.

The CTS implementation uses the slow interfaces for interfacing the keyboards with the processor but uses a high speed display bus for distributing display data. Instead of housing each refresh memory and video generator in the corresponding terminal and connecting to the processor with a slow speed serial data line, all refresh memories and video generators are packaged together and connected to the display bus, allowing high speed parallel data transfers to be made into and out of each terminal's refresh memory. The display bus is connected to the processor bus by an interface unit which effectively makes the display bus an extension of the computer bus. Because of the high speed feature of the data distribution system, data transfers into a terminal's refresh memory need not be made one word at a time. The refresh memory can accept data as rapidly as the processor can output it and, therefore, the processor can output blocks of display data of whatever length is convenient for the display processing task. The Display Controller Subsystem organization is such that the data transmission time required to update all 32 terminals in a cluster is less than 250 milliseconds. The data stored in the refresh memory is converted to a composite video signal requiring only a single high frequency coaxial cable to distribute the video signal to the terminal.

3.1.2 DC Random Graphics

The second unique feature of the Display Controller Subsystem is the technique used to generate random graphics. Unlike CTS, those terminals that use raster (TV type) displays and have random graphic capability incorporate an image memory in which is stored an analog of the display screen, i.e. for every point on the display there is a corresponding location in memory. This is very wasteful of memory since most of the display screen is blank and very little of the image memory is used to store useful information. In the CTS Visual Display Unit (VDU) better utilization is made of the graphic portion of refresh memory than in an image memory system by concentrating memory usage around the screen areas which contain information.

As illustrated in Figure 3-2, the VDU display screen is divided into 50 columns and 30 rows of display cells. Each cell consists of a 9x15 dot

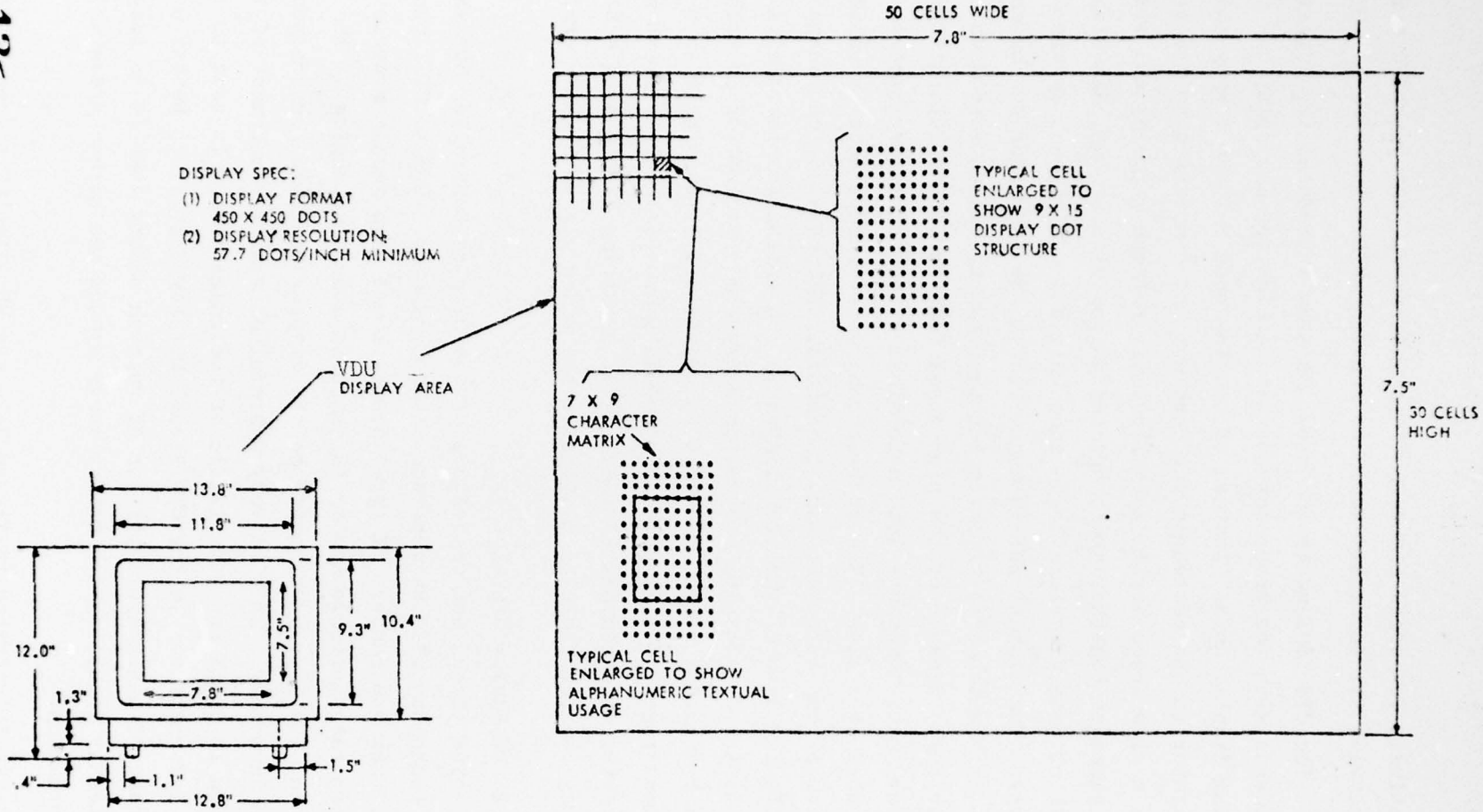

Figure 3-2 VDU Display Area Utilization

matrix. When generating random graphics, the data is examined to determine how many unique 9 x 15 dot patterns are required to produce the desired display. These patterns are then software generated and stored in the graphic portion of the refresh memory. Up to 256 graphic patterns are programmable at a display frame to display frame basis. There is no restriction on the number of times a particular 9 x 15 graphic pattern can be repeated on the display screen other than no more display cells can be used than are available. This technique for generating random graphics uses about 35K bits of storage for the 256 patterns. This compares very favorably with the 202K bits that would be needed if a conventional image memory approach had been implemented. In addition the programmable pattern memory and the 1500 word table have a two way interface with the high speed display bus. Besides accepting data output by the processor, the two sections of refresh memory have the capability, on command, to transmit data back to the processor.

3.1.3 Display Terminals

Terminal stations consist of a keyboard, a VDU, a base for the VDU and a four foot cable to connect the keyboard to the VDU base. The VDU base contains a power supply and a keyboard transceiver. The transceiver interfaces the keyboard and the instructor printer with the processor over a 110 baud line. The power supply provides power to the keyboard and the transceiver.

The DC PDP 11/35-FL computer includes the basic CPU and power supplies, 32K of core memory, a memory management unit, power fail restart, a programmer's console, and 4-level automatic priority interrupt. To this unit are added a teletypewriter controller, a bootstrap loader, a programmable real-time clock, a 1.2 million word disk and disk controller, asynchronous communication multiplexers, and interprocessor links.

The communication multiplexers interface the 32 keyboards and 2 printers in a cluster over 110 baud data lines. The interprocessor links are of two types. The link to the Data Base Controller is a general purpose bus interface which can operate in either a word mode or a block mode. Data transfers between the Display Controller and the System Controller are accomplished using a general purpose program controlled interface (word mode only).

3.2 Data Base Controller Subsystem

The Data Base Controller Subsystem consists of the Data Base Disk Subsystem and the Controller. The Controller is a PDP 11/35-FL computer mainframe consisting of the basic CPU and power supplies, 32K of core memory, a memory management unit, power fail/restart, a programmer's console, and a 4-level automatic priority interrupt. To this unit are added a teletypewriter controller, a bootstrap loader, a programmable real-time clock and five communication interfaces. The five interfaces provide high speed communication links with all other processors in the CTS; transfers can be made one word at a time or in blocks.

The Data Base Disk Subsystem consists of Diva Associate's Model DD-25. This unit is made up of a Diva disk controller and two Century Data CDS-215 disk drives. The Diva controller interfaces the drives with the PDP 11/35 processor. The CDS-215 is a dual-spindle drive that uses the 20 surface, IBM-type, 2316 disk pack. The drive features double density (400 tracks per surface) which enables it to store 58 megabytes per spindle. The four spindles provide storage for 232 megabytes.

3.3 System Controller

The System Controller computer is a PDP 11/35-FL mainframe consisting of a CPU and power supplies, 128K of core memory, a memory management unit, power fail/restart, a programmer's console, 4-level priority interrupt, a teletypewriter controller, a bootstrap loader, a programmable real time clock, a floating point unit, a hardware multiply/divide unit, a programmable stack limit, a disk controller and three disk drives each with a 1.2 million word capacity, a 300 lpm printer, a magnetic tape unit controller and four 9 track tape transports, a card reader/punch terminal and interprocessor links. The links connecting the System Controller to the Display Controllers are program controlled general purpose digital interfaces. The System Controller to Data Base Controller link is a bus interface which can operate in either the word or block transfer mode.

4.0 Installation

The original CTS specification was for the installation of the equipment in Squier Hall at Fort Monmouth, N.J. Later, this requirement was amended to change the site to Fort Gordon, Ga. Since, the final location of the Ft. Gordon classrooms was unknown, the CTS contract was negotiated on the basis that the Fort Gordon installation would be identical to that

initially specified. Subsequently, the CTS contract was modified to include an installation study whose purpose was to determine the most effective and economical method of implementing the Army's Ft. Gordon installation plan when it was finalized.

The Fort Monmouth site allowed all equipment to be located in the same building with the distance separating a terminal from its associated Display Controller not exceeding 500 feet. The Fort Gordon installation has a central computer room in Moran Hall and terminals distributed at various locations within Moran, Greely and Brant Halls. Besides being located in buildings separate from the central computer room, the terminals in Greely and Brant Halls are remoted from the Display Controllers by a distance greater than the 500 foot capability initially designed into the system. After discussions on the alternatives for implementing the longer distances, the Army decided to keep all display generation and computer equipment in Moran Hall and find a method of driving the long cable lengths connecting the video generator outputs to the remote terminals.

As part of the study, laboratory tests and on site experiments in the actual operating environment were conducted to determine the effects of long video and communication lines, the adequacy of electrical grounding between buildings, the need for video amplification and equalization and the need for communication transmission equipment. Besides these experiments, recommendations were made as to equipment and cable selection, and patch and disconnect panel requirements.

The Brant Hall video circuit configuration recommended to the Army and then implemented is shown in Figure 4-1. The isolation transformers provide protection from ground loops and spurious signals; the video amplifier and equalizing stub provide the restoration of the display to acceptable performance levels. In the Greely Hall installation, isolation transformers were required but not the video amplifier and equalizing stub because the distances are shorter than in Brant Hall and there is less distortion in the video pulse. In Moran Hall, no transformers, amplifiers or stubs were required.

The Army's installation plans called for direct burial of the cables interconnecting the equipments in Moran Hall with the terminals in Brant and Greely Halls. As part of the installation study, recommendations were

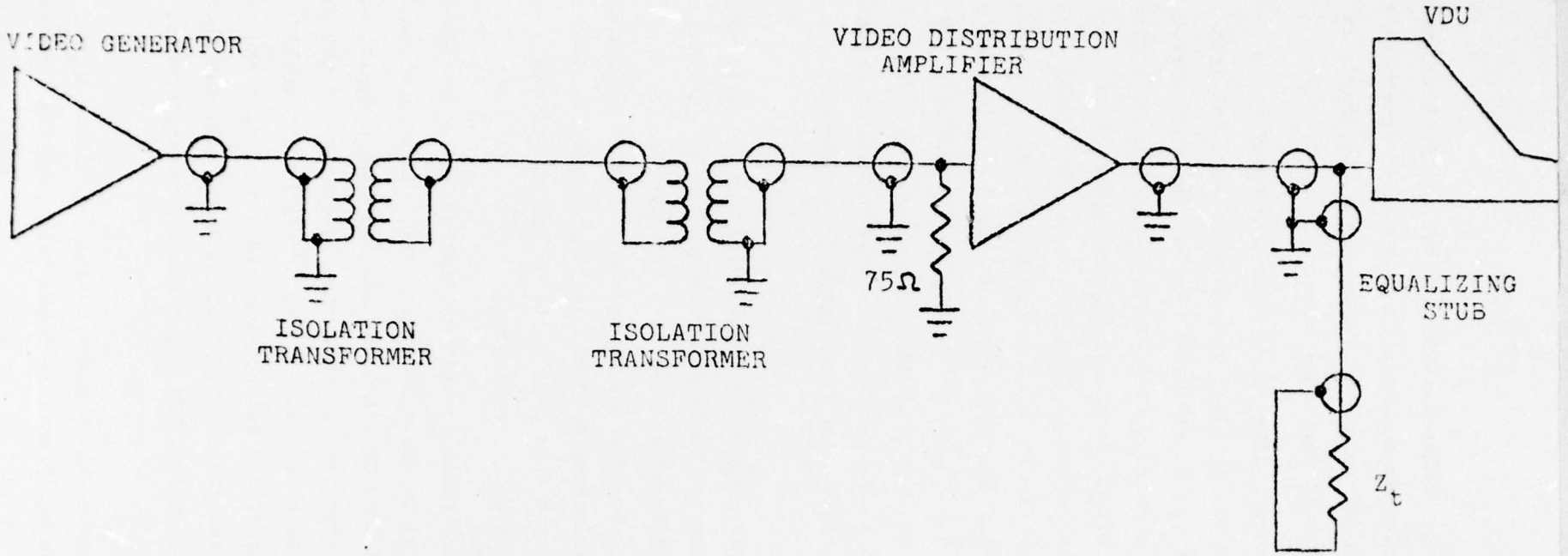

Figure 4-1

Brant Hall Video Circuit Configuration

made on cable types suitable for direct burial. One of these, a modified RG12 A/U, was selected by the Army for the video circuits. This cable has the electrical characteristics of RG11, is impregnated with a water and vapor impermeable layer and has an outer steel tape armor for rodent protection. The selected data cables contain 40 individually shielded twisted pairs, are impregnated for water and vapor protection and have a steel armor. Details of the installation study are given in the Installation Study Technical Report, dated June 1975.

Based on the results of the installation study and subsequent discussions and negotiations the CTS contract was modified to include the installation task. The 128 CTS circuits, where a circuit contains a video and a 110 baud data communication line, are terminated at the Master Patch Panel located in the same room as the central computer equipment in Moran Hall. The Master Patch Panel allows any of the 128 incoming circuits to be manually patched to any of 200 outgoing circuits. Each of the 128 terminals is equipped with a disconnect panel where video and communication cables terminate and to which the terminal's video and communication cable can be connected to pick up the appropriate signals.

5.0 CTS Software

GTE Sylvania's software system is designed to accommodate the real time multi-user environment required for CTS. In addition, it is a general purpose system which is capable of servicing multiple non-real time tasks concurrently with real time activities or in a stand alone configuration.

The complete CTS software consists of the following major programs.

System Controller
Display Controller
Data Base Controller
Class I Language Assembler
Sort/Merge
System Readiness Checkout
DEC RSX-11D Version 6B Executive
DEC PDP-11 Series software utilities

These programs were implemented as described in "Computerized Training System Design Plan" dated 28 January 1974 and revised 28 February 1974

with the exception of the modifications and enhancements that are described in the following sections. A brief description of CTS is provided in the document "CTS System Level Summary".

5.1 System Controller

The software executed at the SC consists of

1 - DEC RSX-11D Executive Operating System and its associated utility programs as described in the DEC RSX-11D Manuals,

2 - Sort/Merge program as described in the document "Sort-11 Users Manual", and

3 - CTS associated tasks as described in the following CTS Program Unit Specification Documents

DCIRTE Task
DBCDMA, DCIOOØALL, and ADMINT Tasks
STUDENT, INSTRC Tasks
SYSPRG Task
EDITOR Task
Class I Compiler Task
General Subroutines
DR11C and DA11B Driver Tasks

Additional CTS information is also provided in the following user documents:

Instructional Programmer Editor Users Manual
System Programmer User Manual
System Programmer Reference Manual
CLASS I Compiler Users Manual
CLASS I Compiler Reference Manual

Operation of CTS is controlled from the SC operator's console. Operator functions are described in the document "CTS Computer Operator's Manual".

SC modifications and enhancements are described in the following sections.

5.1.1 RSX-11D Operating System

The original delivery of CTS operated under control of the DEC RSX-11D Operating System Version 4A. Tests indicated that version 4A was not adequate to handle peak traffic loads of 128 users. To correct this condition, the latest version of RSX-11D, Version 6B, was implemented. This version

has a much improved file handling capability and a much larger dynamic storage area. Subsequent tests, simulating extremely heavy traffic loads, proved that Version 6B is capable of supporting the CTS traffic requirements.

5.1.2 SAVESR Task

A new CLASS I Compiler command, SAVESR, for saving student data on magnetic tape at the SC was implemented during the Phase II tests to illustrate the technique for adding new commands to the CLASS I Language. This command was then officially incorporated into the CLASS I Language to be processed as part of Student processing by the STUDNT task at the SC. Depending on the frequency of use and amount of data saved, tests indicated that the STUDNT task could not process this data fast enough to prevent saturation of the RSX-11D node pool. To correct this condition a separate task, named SAVESR, was written just to handle this data. By running SAVESR at a very high priority, the saturation problem was eliminated. A sense-switch test was also included to allow optional collection of student data and to provide for operator recovery of magnetic tape problems or changing tapes.

5.1.3 LOGONF Task

User log on and log off were originally part of the DC input routing task DCIRTE. As such, log on/off requests were processed along with other DC inputs on a first in first served basis. In addition, a data file search was required to service and validate the log on requests. As a result, the average log on time was six seconds. In the operating environment envisioned by the customer, i.e., a Computer Managed Instruction (CMI) where users are loging on and off frequently, this log on delay was too long. As a result, the log on/off function was removed from DCIRTE and installed as a separate task, LOGONF. In addition, user ID and password information is initially read from disk, sorted and stored in computer memory. An incore binary search is then performed at log on time rather than a sequential disk search. These changes reduced log on time to one second.

5.1.4 PWRUP Task

To satisfy the warm start and power fail recovery requirements of CTS, a power fail recovery task, PWRUP, was written. This task is executed from the SC and is used to restart a Display Controller that has halted for any reason, i.e. power fail, hardware failure, or deliberate halt. It

reloads the DC with instructor data and restarts each student user from his last restart point. Since student log on data is also stored on the SC disk, recovery is also possible in case of an SC problem requiring a new SC reboot from disk. A description of this task is provided in the document "PWRUP Task".

5.1.5 SYSPRG Task

Three enhancements were made to the System Programmer task, SYSPRG. The command SYSTAT was changed to display summary CTS system status information for each user type by DC. A new command, SENDSP, was included to allow messages to be sent from the SC operator console to any, or all, terminal stations. The third modification was to the DELUNT command for deleting lesson units from the DBC. A test is now made that will prevent deleting a lesson unit that is currently being used by a student. This test was incorporated to preserve the validity of the student's restart record.

5.1.6 BIGED Task

Two versions of the IP Editor task were installed. Task BIGED supports up to 12 concurrent IP's while task EDITOR supports only six. Task EDITOR represents a savings of over 3K of memory over BIGED.

5.1.7 DCIRTE Task

As discussed in 5.1.3, the log on/off function was removed from task DCIRTE and installed as a separate task, LOGONF. As a result, the functions of DCIRTE were reduced to the point where they could be handled by the DR11C device driver tasks AX, BX, CX, and DX. This provided a significant memory savings by removing DCIRTE and also reduced the demands on the RSX-11D node pool resulting in faster execution of DC input requests.

5.1.8 CLASS I Compiler Task

Two new commands were added to the CLASS I compiler and the processing of one command was modified to accommodate the way in which it is used by the Army. The two new commands are SAVESR, as described in 5.1.2, and LOGOFF. The LOGOFF command allows the course author to force a student user to be logged of CTS at that point in the lesson. Implementation of the LOGOFF command required an associated modification to the DC program.

The modified command is COMMON. Implementation of the COMMON command requires that it can only be preceded by a NOTE command or another COMMON command. To use a subroutine, or a MACRO, to specify the common area, it was necessary to change COMMON Command processing to perform special handling of the commands SUBRTN, RETURN, SEND and CALL.

5.2 Display Controller

The function of the DC is to respond to and service, or initiate service for, all keyboard input requests from each of its 32 terminal stations. A terminal station may be occupied by a student, an instructor, an IP or an administrator. It processes all student and instructor requests that it can and sends the remainder to the SC for processing. All IP and administrator requests are sent to the SC for processing. By allocating DC resources in this way, the specified one and two second student response time delay is controlled. The DC software is documented in "Program Unit Specifications for the Display Controller." A description of the instructor commands is contained in "CTS Instructor's Manual."

DC modifications and enhancements are described in the following sections.

5.2.1 Student Look ahead technique

When the DC program disk storage requirements became more closely defined, it was possible to increase the disk area used to store a student's lesson material from 12K to 22K words. For a maximum size lesson unit of 64K, this means that one third of a lesson unit can be stored at the DC at any given time. The 22K words are divided into eleven 2K blocks to match the 2K buffer size used for DC/DBC communications. The DC lesson data 2K block #N is replaced with a new data block, # N+11, when the material in data block #N+4 is executed. For example, when data block #5 is executed, data block #12 will be requested from the DBC, and will replace data block #1 on the DC disk. Implementation of a larger disk area at the DC, increases the probability that the needed student lesson data is available on the DC disk, and, hence, helps to reduce the student response time delay.

5.2.2 Home and Highlight Keyboard Keys

To enhance terminal keyboard capability, a cursor home key and a character highlight key were implemented. The HOME key allows a user to position the keyboard cursor that is displayed on the VDU to the home

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position, row one column one, on the VDU via a single keying stroke. The highlight key allows the user to display any of the 96 ASCII characters in a video inverted mode, i.e., dark character on a light background, directly from the keyboard. Initially, this capability was available only through the CLASS I WRITE command.

5.2.3 Power Fail Recovery/Restart Record Handling

A power fail recovery routine was written that initializes the DC to receive recovery data from the SC power recovery routine described in section 5.1.4. To effectively use the power recovery feature, student restart record processing was modified. Instead of holding the last restart record at the DC and sending it to the DBC only at log off, the restart record is sent to the DBC every time a new restart point is reached. In this way, the most recent restart record is obtained from the DBC in case of a DC power fail recovery.

5.2.4 Student Scratch Buffers

Analysis indicated that student response time would not be noticeably affected if the number of 1K scratch buffers, used by student lessons, was reduced from four to two. This resulted in a 2K savings in memory at each DC.

5.3 Data Base Controller

The function of the DBC is to maintain the lesson units and student restart records stored on the disks at the DBC. It communicates with the SC and each DC and processes their requests for data. A complete description of the DBC programs is contained in the document "Program Unit Specifications for the Data Base Controller".

DBC modifications and enhancements are described in the following sections.

5.3.1 Power Fail Recovery

A power fail recovery program routine was written that boots in a new copy of the DBC program upon power resumption after a power failure. This reinitializes the DBC in a manner analogous to the SC and DC and readies it for the power recovery process.

5.3.2 Directory Dumps

Additional DBC directory dump routines were provided. These routines were developed as a debugging aid for the DBC programs during development. They were subsequently tested and supplied to the Army as part of the DBC program package. These dumps provide more detailed data on the lesson units and restart record directories than is listed via the System Programmer DIRECT Command. These directory dumps are detailed in Appendix A of the DBC Program Unit Specification Document.

5.4 System Readiness and Checkout

The CTS Readiness Test program provides a profile of the system hardware status by determining and reporting, for each unit of peripheral equipment, whether that unit is in a 'go' or 'no-go' state. Another function is to initiate the loading of the main CTS operational programs at the SC, DBC and DC's and to pass device status information to these programs. The tests are not designed to be exhaustive diagnostics. A description of the System Readiness Test programs is contained in the document "Program Unit Specifications for the System Readiness and Checkout Programs". Use of these programs is described in the CTS Operator's Manual.

5.5 Initial System to Final System File Conversion

Data files generated on the CTS Initial System are not directly compatible for use on the CTS Final System. A procedure for converting these files and the associated programs are described in document "CTS Initial System to Final System File Conversion Manual".

6.0 Acceptance Tests

6.1 Phase I

Phase I acceptance testing was completed on the Initial System at Ft. Gordon, Ga in September of 1974.

6.2 Phase II

Phase II testing was performed at the GTE Needham facility using the System Controller, Data Base Controller and three Display Controllers operating 40 terminals. The tests were completed in April 1975.

6.3 Phase III

Phase III testing of the full 128 terminal system was completed in July 1976. A list of software discrepancies was submitted by the Army.

These discrepancies were corrected and detailed in a report titled "CTS Test and Demonstration Report Phase III Test" dated 15 October 1976.

7.0 Summary and Conclusions

The Computerized Training System shown in Figure 1-1 is a low cost, high speed, CAI/CMI training system containing many desirable features which make it readily adaptable to most any configuration desired. The CTS was designed to support five user types and to provide a fast response to student requests. To this end a system of six minicomputers was chosen for the 128-terminal system. Four of these computers are Display Controllers, each servicing up to 32 CAI terminals. All Display Controllers are configured identically with the same software package operating in each. The other two computers are the System Controller and the Data Base Controller. Rapid student response time is obtained by assigning sufficient capability to the Display Controller so that it can process most student requests. Users with less demanding response criteria, i.e., Instructional Programmers and Administrators, have their requests transmitted to the SC for processing.

The System Controller is the system executive for CTS and it services and processes inputs from each of the four DCs and initiates data requests to the DBC. It contains an Editor function and Class I Language Assembler for use by the IPs and processes student requests that the DC cannot handle. It also validates and processes all System Programmer commands.

The Data Base Controller has responsibility for maintaining the CTS course material data base. It stores and retrieves data for the SC and the DCs. By relieving the SC of the overhead required to service such a large data base, the SC is better equipped to perform its assigned tasks. The overall effect of the DBC is improved response time in the SC and DCs. A large Data Base Disk Subsystem is provided by Diva Associate's Model DD-25. This unit is capable of storing 232 megabytes of data.

In addition to an efficient system organization, critical factors which make it possible to meet the fast response time requirements to student requests are inherent in the design of the display refresh memory and the communications link connecting the display generation equipment to the Display Controller. To meet the specified response time requirements, a

high speed interface between the display generation equipment and the Display Controller was essential. GTE Sylvania provides the essential high speed interface by using a 2-way electronic bus interface which ties the display terminal directly to the Display Controller minicomputer bus.

Some of the many desirable features and capabilities provided by the CTS are briefly listed below:

1) Lesson material can be entered via any of the CAI terminals using the CTS Language Commands provided.

2) Alphanumeric, fixed and programmable graphic capabilities are provided at each CAI terminal.

3) The system is capable of cold and warm start operation.

4) Each minicomputer is capable of detecting power failure and initiating procedures to save volatile registers and memory. The return of power to a safe operating level initiates restart and transfer of control to the operational program(s).

5) Each student terminal has the capability of independently accessing any lesson in the system.

The software system delivered by GTE Sylvania is a fully integrated package designed to accommodate the real-time multi-user environment required for the CTS. In addition, it is a general purpose system which is capable of servicing multiple non-real time tasks concurrently with real-time activities or in a stand-alone configuration.

8.0 Recommendations

CTS was initially designed for an installation where terminals were to be located fairly close to the computers. Later, the system was modified to permit remoting terminals in nearby buildings. Other system configurations can be conceived which would totally eliminate restrictions on the distance between terminals and computer. Two of these are discussed: An intelligent stand alone terminal configuration and a remoted Display Controller configuration. A very high speed CTS is also described.

8.1 Stand-Alone Terminal

Maximum flexibility can be obtained by creating a stand-alone intelligent terminal which can operate independently of the rest of the system.

Such a terminal could be located virtually anywhere without incurring any exhorbitant installation costs. Figure 8-1 illustrates a stand-along terminal configuration. The central item is an LSI-11 microcomputer which contains the central processor, memory and an I/O bus port on one printed circuit card. The LSI-11 can execute an instruction set comparable to that of the PDP-11/35 at speeds equivalent to that of the PDP-11/05.

To the LSI-11 microcomputer would be added a bootstrap loader, an interface to the keyboard and to the display generation equipment, and a small low cost disk drive for lesson material and program storage. An interface to allow the terminal to communicate with the rest of the system over a telephone line could also be added, giving the added flexibility of changing lesson material by way of the telephone link as well as by changing the disk cartridge. As an additional feature, the intelligent terminal controller could be designed to handle a small cluster of terminals.

8.2 Remote Display Controller

Remoting the Display Controller as well as the terminals allows nearly unlimited separation between the DC and the central computer installation. As shown in figure 8-2, all communications between the remote DC and the central computer complex would be over one high speed dedicated line. Modem interfaces and Bell 303 equivalent modems would be added to the remote DC and to the DBC. Also, software would be added to these two controllers to handle the communications interface. In this configuration, the DBC handles all communication with the remote DC since there is no direct link between the SC and remote DC. By increasing the capacity of the local disk to the point where it is large enough to store all lesson material needed at the remote location, the high speed modems and dedicated line could be replaced by a telephone line and a low speed modem or they can be eliminated. If the link is eliminated, lesson material could be changed by simply changing the disk cartridge. By removing this link back to the DBC, a mobile, van-mounted training center can be conceived.

8.3 High Speed System

Overall system response times of the present system configuration can be improved by using Digital Equipment Corporation (DEC) PDP-11/45 minicomputer with a cache memory option.

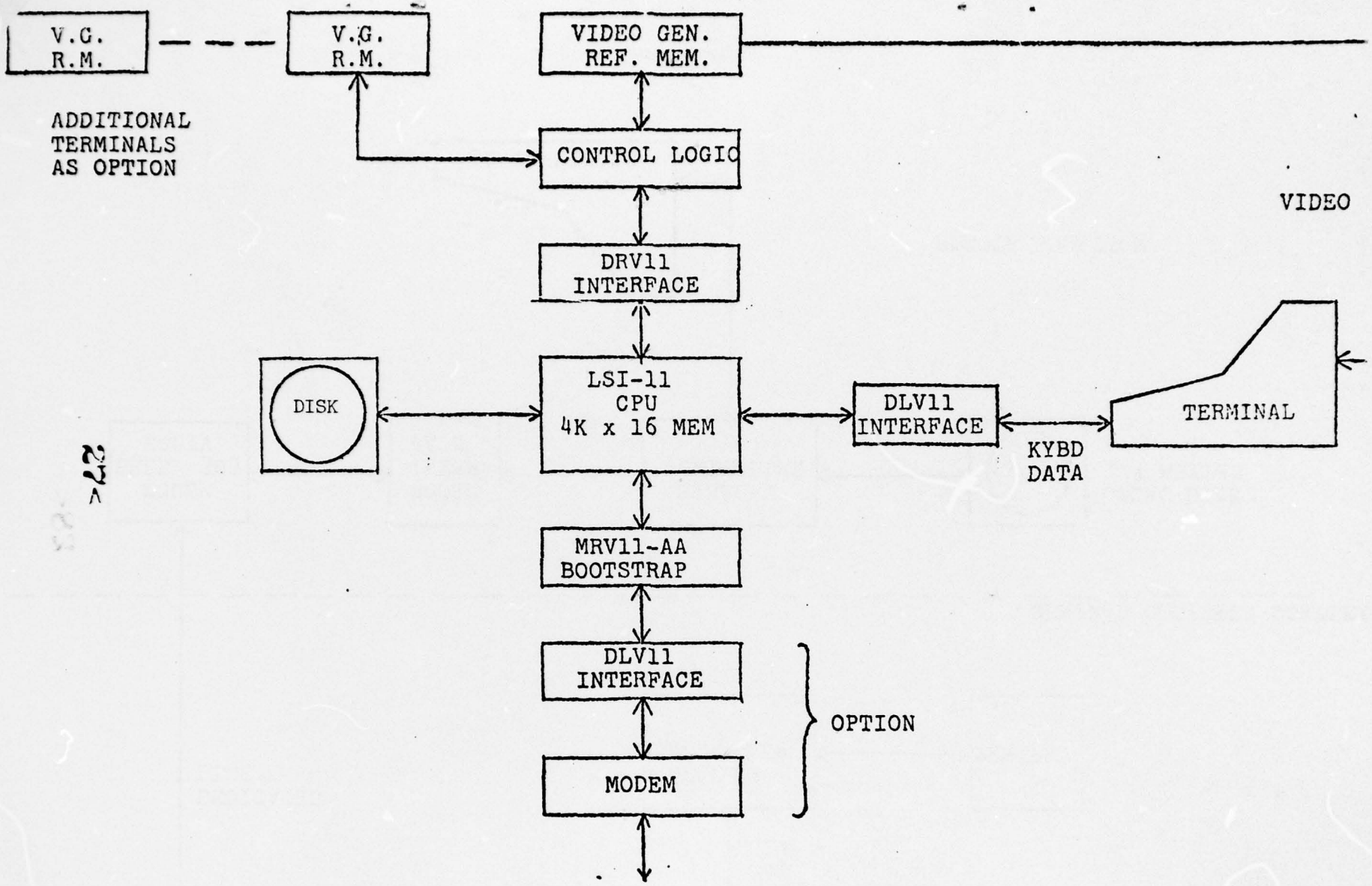

Figure 8-1 Block Diagram of Stand Alone Terminal

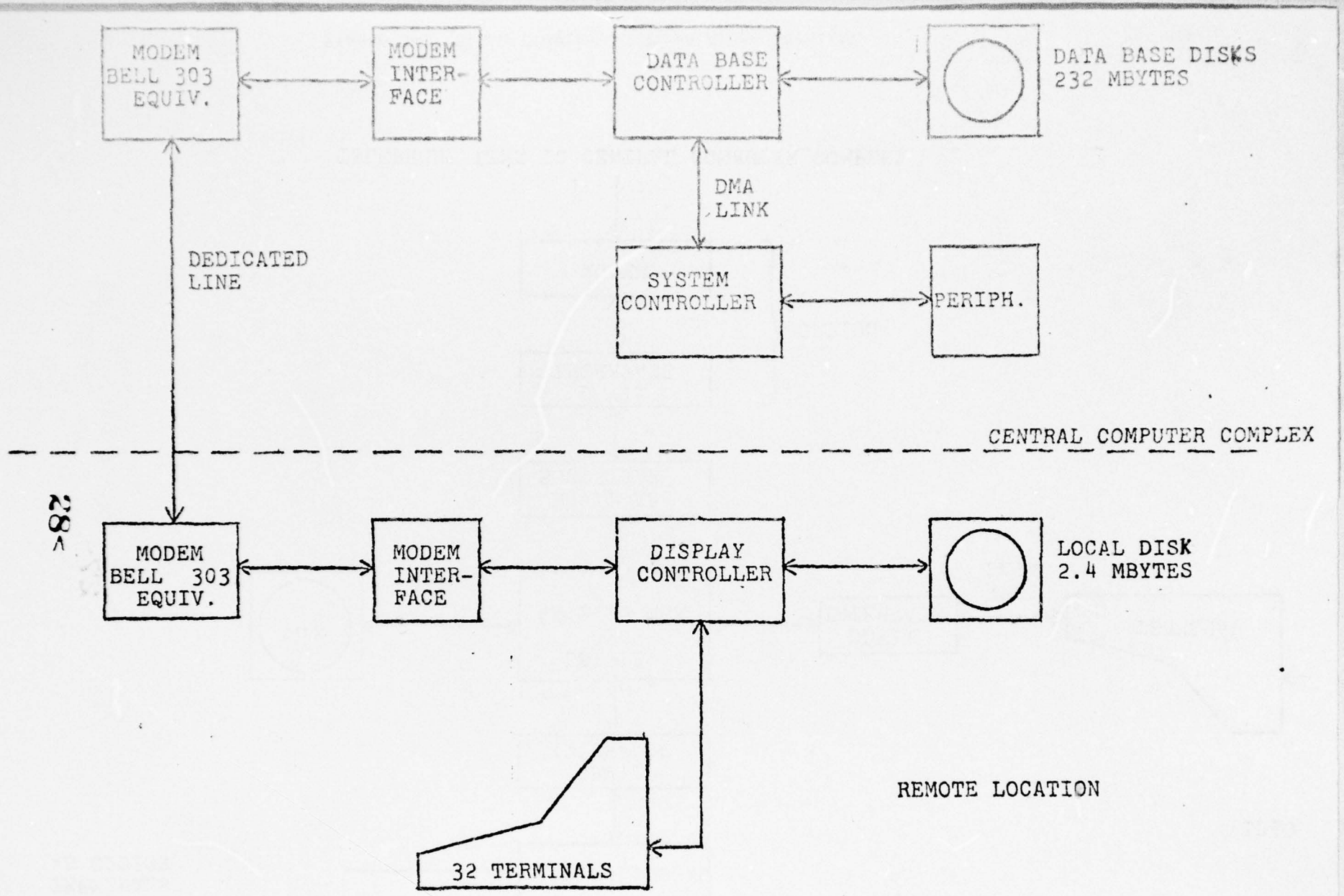

Figure 8-2 Remote Display Controller

The PDP-11/45 is a powerful 16-bit minicomputer designed as a computational tool for high-speed real-time applications and for large multi-user, multi-task applications. It will operate with solid state and core memories up to 124K words. The CPU has a cycle time of 300 nanoseconds and performs all arithmetic and logical operations required in the system.

Four types of memories can be freely mixed and interchanged in the PDP-11/45 to best suit the user's needs. The programmer need not address all of his solid state memory consecutively, but he can intermix solid state and core physical addresses thus providing an additional degree of freedom. The four types of memory available are as follows:

SOLID STATE:

1) Bipolar Memory with a cycle time of 300 nsec
2) MOS Memory with a cycle time of 495 nsec

CORE:

1) 8K increments with a cycle time of 900 nsec
2) 16K increments with a cycle time of 980 nsec

Selective intermixing of solid state and core memories will provide the user with faster program execution speed but only in those areas where solid state memory is incorporated.

From a cost effectiveness standpoint, a cache memory system offers faster system speed for the cost of only a small quantity of fast memory plus associated logic. How much faster depends on the size of main memory. The user receives a very substantial speed improvement for a modest cost, and the operation is transparent to the user.

A cache memory is a small, high-speed memory that maintains a copy of automatically selected portions of main memory for faster access to those instructions and data used most often by the system. A computer system, using a cache memory, appears the same as a conventional system with core memory, except that the execution of programs is noticeably faster. Other semiconductor-core systems attempt to achieve this goal by having the programmers guess ahead of time which sections of the program should go in which memory. The cache system achieves the same goal by automatically, dynamically shuffling data between the two memory types in a way which gives a high probability that useful data will be in the fast memory.

To complement this high speed system, high speed local disk drives and controllers should be used. In addition, increasing the present storage capacity of the Display Controller disk subsystem could allow all student lesson material to be stored locally at the Display Controller thus providing an added improvement in system response times. The larger disk storage capacity could also be used to capture more student and terminal data.

8.4 Lightning Protection

At the time that the installation study was performed by GTE Sylvania, it was recommended that lightning protection be built into the cabling and video/signal distribution system that connects the central computer complex to the classroom terminals. Due to economy reasons, this protection was not included in the remote installation system, and lightning has caused damage to transistors at the cable interface, and in turn delays to the full testing of CTS. It is recommended that to achieve the reliability needed for Signal School operation, protection circuits be installed at the earliest opportunity.